



[Home](#) | [Login](#) | [Logout](#) | [Access Information](#) | [Alerts](#) |

Welcome United States Patent and Trademark Office

❑ Search Results

BROWSE

SEARCH

IEEE XPLORE GUIDE

Results for "((soc verification)<in>metadata)"

Your search matched **14** of **1192192** documents.

A maximum of **100** results are displayed, **25** to a page, sorted by **Relevance** in **Descending** order.

 e-mail

» [View Session History.](#)

» New Search

Modify Search

» **Key**

```
((soc verification)<in>metadata)
```

IEEE JNL IEEE Journal of
Magazine

☐ Check to search only within this results set

IEE JNL IEE Journal or Magazine

Display Format: ☒ Citation ☐ Citation & Abstract

IEEE
CNF IEEE Conference
Proceeding

Select Article Information

IEE CNF IEE Conference
Proceeding

1. **Reuse issues in SoC verification platform**
Rui Wang; Wenfa Zhan; Guisheng Jiang; Minglun Gao; Su Zhang;
Computer Supported Cooperative Work in Design, 2004. Proceedings. The 8th International Conference on Computer Aided Design and Computer Graphics, 2004. Volume 2, 26-28 May 2004 Page(s):685 - 688 Vol.2
AbstractPlus | Full Text: PDF(497 KB) IEEE CNF

IEEE
STD IEEE Standard

2. **Formal verification of a system-on-chip using computation slicing**
Sen, A.; Bhadra, J.; Garg, V.K.; Abraham, J.A.;
Test Conference, 2004. Proceedings. International
2004 Page(s):810 - 819
[AbstractPlus](#) | [Full Text: PDF\(1032 KB\)](#) [IEEE CNF](#)


3. Nuts and bolts of core and SoC verification
Albin, K.;
Design Automation Conference, 2001. Proceedings
2001 Page(s):249 - 252
AbstractPlus | Full Text: PDF(324 KB) | IEEE CNF

4. IP reuse creation for system-on-a-chip design
Bricaud, P.J.;
Custom Integrated Circuits, 1999. Proceedings of the IEEE 1999
16-19 May 1999 Page(s):395 - 401
[AbstractPlus](#) | [Full Text: PDF\(604 KB\)](#) | [IEEE CNF](#)

5. Twelfth Annual IEEE International ASIC/SOC Conference (Cat. No.99TH8454)
ASIC/SOC Conference, 1999. Proceedings. Twelfth Annual IEEE International
15-18 Sept. 1999
AbstractPlus | Full Text: PDF(36 KB) IEEE CNF

6. Predicting the performance of SoC verification technologies
Peterson, G.D.;
VHDL International Users Forum Fall Workshop, 2000. Proceedings
18-20 Oct. 2000 Page(s):17 - 24
AbstractPlus | Full Text: PDF(500 KB) IEEE CNF

7. A system verification environment for mixed-signal SOC design based on IP bus

- ┐ Zhang Yuhong; He Lenian; Xu Zhihan; Yan Xiaolang; Wang Leyu;
ASIC, 2003. Proceedings. 5th International Conference on
Volume 1, 21-24 Oct. 2003 Page(s):278 - 281 Vol.1
[AbstractPlus](#) | Full Text: [PDF\(308 KB\)](#) IEEE CNF
- ┐ **8. Current status and challenges of SoC verification for embedded systems market**
Wooseung Yang; Moo-Kyeong Chung; Chong-Min Kyung;
SOC Conference, 2003. Proceedings. IEEE International [Systems-on-Chip]
17-20 Sept. 2003 Page(s):213 - 216
[AbstractPlus](#) | Full Text: [PDF\(406 KB\)](#) IEEE CNF
- ┐ **9. Symbolic simulation as a simplifying strategy for SoC verification**
Dumitrescu, E.; Borriane, D.;
System-on-Chip for Real-Time Applications, 2003. Proceedings. The 3rd IEEE Internat
on
30 June-2 July 2003 Page(s):378 - 383
[AbstractPlus](#) | Full Text: [PDF\(303 KB\)](#) IEEE CNF
- ┐ **10. On-chip stochastic communication [SoC applications]**
Dumitras, T.; Marculescu, R.;
Design, Automation and Test in Europe Conference and Exhibition, 2003
2003 Page(s):790 - 795
[AbstractPlus](#) | Full Text: [PDF\(342 KB\)](#) IEEE CNF
- ┐ **11. Automatic hardware-efficient SoC integration by QoS network on chip**
Bolotin, E.; Morgenshtein, A.; Cidon, I.; Ginosar, R.; Kolodny, A.;
Electronics, Circuits and Systems, 2004. ICECS 2004. Proceedings of the 2004 11th IE
Conference on
13-15 Dec. 2004 Page(s):479 - 482
[AbstractPlus](#) | Full Text: [PDF\(867 KB\)](#) IEEE CNF
- ┐ **12. SoC Verification**
Duen-Jeng Wang; Narayan, S.;
ASIC/SOC Conference, 1999. Proceedings. Twelfth Annual IEEE International
15-18 Sept. 1999 Page(s):25 - 26
[AbstractPlus](#) | Full Text: [PDF\(24 KB\)](#) IEEE CNF
- ┐ **13. FlexBench: reuse of verification IP to increase productivity**
Stohr, B.; Simmons, M.; Geishauser, J.;
Design, Automation and Test in Europe Conference and Exhibition, 2002. Proceedings
4-8 March 2002 Page(s):1131
[AbstractPlus](#) | Full Text: [PDF\(177 KB\)](#) IEEE CNF
- ┐ **14. Verification strategy for integration 3G baseband SoC**
Mathys, Y.; Chatelain, A.;
Design Automation Conference, 2003. Proceedings
2-6 June 2003 Page(s):7 - 10
[AbstractPlus](#) | Full Text: [PDF\(494 KB\)](#) IEEE CNF
- 

[Home](#) | [Login](#) | [Logout](#) | [Access Information](#) | [Alerts](#) |

Welcome United States Patent and Trademark Office

☐ Search Results[BROWSE](#)[SEARCH](#)[IEEE XPLORE GUIDE](#)

Results for "(soc validation<in>metadata)"

☒ e-mail

Your search matched 1 of 1192192 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

[» View Session History](#)[» New Search](#)[» Key](#)

IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

Modify Search

☐ Check to search only within this results setDisplay Format: ☒ Citation ☐ Citation & Abstract

- ☐
1. **System-on-chip validation using UML and CWL**
Zhu, Q.; Oishi, R.; Hasenawa, T.; Nakata, T.;
Hardware/Software Codesign and System Synthesis, 2004. CODES + ISSS 2004. Inte
Conference on
2004 Page(s):92 - 97
[AbstractPlus](#) | Full Text: [PDF\(478 KB\)](#) IEEE CNF

Indexed by

[Help](#) [Contact Us](#) [Privacy &](#)

© Copyright 2005 IEEE -